2815

PTO/SB/21 (05-03)
Approved for use through 04/30/2003. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/467,141
Filing Date	December 10, 1999
First Named Inventor	Ma, Yueh Yale
Art Unit	2815
Examiner Name	Eugene Lee
Total Number of Pages in This Submission	8
Attorney Docket Number	020487-000300US

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☒ Amendment/Reply
  - ☐ After Final
- ☐ Affidavits/declaration(s)
- ☒ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s)
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to Group (Appeal Notice, Brief, Reply Brief)
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below)*:
  Return Postcard

Remarks	The Commissioner is authorized to charge any additional fees to Deposit Account 20-1430.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual	Townsend and Townsend and Crew LLP
	Barmak Sani Reg. No. 45,068
Signature	
Date	May 23, 2003

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Typed or printed name	DJ Bogorodsky		
Signature	DJ Bogorodsky	Date	May 23, 2003

PA 3307407 v1

#16 Response to Notice of Non-Compliance 6/3/03

PATENT

Attorney Docket No.: 020487-000300US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Examiner: Eugene Lee
Yueh Yale Ma et al.	Art Unit: 2815
Application No.: 09/467,141	
Filed: December 10, 1999	AMENDMENT
For: DUAL-BIT DOUBLE-POLYSILICON SOURCE-SIDE INJECTION FLASH EEPROM CELL	

Assistant Commissioner for Patents
Washington, D.C. 20231

Date: May 23, 2003

Sir:

In response to the Office Action mailed January 23, 2003, the Applicants provide the following remarks:

REMARKS

Claims 1-18, 21-29, and 37 are pending. Claims 1-4, 7-18, and 25-26 are rejected under 35 USC 103(a) as being unpatentable over Kohda et al. (USPN 5,021,999) in view of Tigelaar (USPN 5,273,926). Claims 5, 6, 21-24, 27-29, and 37 are rejected under 35 USC 103(a) as being unpatentable over Kohda et al. in view of Tigelaar and Guterman (USPN 5,153,691). These rejections are respectfully traversed.

Independent claim 1 is direct to a cell structure while independent claim 28 is directed to a memory array. However, each of these independent claims distinguishes over Kohda et al. and Tigelaar taken singly or in combination at least by reciting "the select-gate ... extending across the entire length of each of the first and second junctions".

The Examiner indicates that although Kohda discloses many of the features of claims 1 and 28 Kohda fails to disclose the above-cited feature of each of

claims 1 and 28. The Examiner attempts to overcome this deficiency by referring to Fig. 3e of Tigelaar et al. which shows control gate 90 extending over source region 74 and drain region 76. It is respectfully submitted that the Examiner fails to provide a proper motivation for modifying Kohda as taught by Tigelaar et al. in the manner suggested by the Examiner. Further, combining Kohda with Tigelaar et al. in the manner suggested by the Examiner renders Kohda unsatisfactory for its intended purpose.

With respect to the motivation for the modification of Kohda, the Examiner indicates that it would have been obvious to one of ordinary skill in the art to modify the vertically-extending control gate 6 in Fig. 3B of Kohda to extend horizontally over the drain and source regions 2, 3 as taught by Tigelaar et al "in order to form a column line that can access the memory cells of an array" (end of paragraph 3 of the Office Action). As support for this assertion, the Examiner refers to column 5, lines 33-36 wherein Tigelaar et al. state:

> Control gates 90 as shown in Fig. 5e correspond to the column lines 16 shown in Fig. 1, while the source and drain regions 74 and 76 correspond to the row lines 12.

It is respectfully submitted that the patent draftee of the Tigelaar et al. patent mistakenly matched up control gates 90 in Fig. 5e with column lines 16 in Fig. 1 instead of with row lines 12, and conversely mistakenly matched up source and drain regions with row lines 12 instead of column lines 16. This appears to be merely a drafting error. It is notoriously well known in this art that in semiconductor memory arrays (e.g., array 10 in Fig. 1 of Tigelaar et al. and array 10 in Fig. 6 of Kohda), gates of memory cells form row lines which are coupled to a row decoder (e.g., to row decoder 14 in Fig. 1 of Tigelaar et al. and to row decoder 12 in Fig. 6 of Kohda), and drain and source regions of memory cells form column lines which are coupled to a column decoder (e.g., to column decoder 18 in Fig. 1 of Tigelaar et al. and to column decoder 14 in Fig. 6 of Kohda). Thus, in both Kohda and Tigelaar et al. the control gates form row lines which serve the same purpose of providing access to the memory cells of the arrays. Thus, it is respectfully submitted that the motivation for modifying Kohda set forth by the

Examiner is improper since control gate 6 of Kohda serves the purpose of providing access to the memory cells without the need to modify it in any way.

Even if a proper motivation for modifying Kohda in the manner suggested by the Examiner could be identified, combining Kohda with Tigelaar et al. in the manner suggested by the Examiner renders Kohda unsatisfactory for its intended purpose. The modification proposed by the Examiner is to extend control gate 6 in Fig. 3B of Kohda horizontally rather than vertically such that control gate 6 extends over the drain region 2 and source region 3. This modification of Kohda renders the memory cell unsatisfactory for its intended purpose for at least two reasons.

First, extending control gate 6 over drain and source regions 2, 3 prevents column lines (bitlines) from contacting the drain and source regions. Kohda extends control gate 6 vertically, in part, to make surface areas of the drain and source regions exposed so that column lines can make contact with the drain and source regions. This is more clearly shown in Fig. 7 wherein Kohda uses bitlines BL1-BL5 to make contact to a common source region and common drain region between every two adjacent cells along each row of cells. If control gate 6 was extended horizontally to cover the source and drain regions as suggested by the Examiner, contact could not be made to the source and drain regions. This not only prevents supplying the proper biasing to program, erase, or read the cell, but also prevents forming the particular array architecture shown in Fig. 7. Kohda achieves its primary goal of storing tri-level data (see Title, Abstract, and Field of the Invention) by incorporating the cell in Figs. 3A, 3B in the specific array architecture shown in Fig. 7. This array architecture is designed to supply the requisite biasing to the array for storing tri-level data in the memory cells. By eliminating the ability to directly contact the common source and common drain regions with the bitlines, the required biasing for storing tri-level data can not be provided to the cells. Therefore, modifying the cell as suggested by the Examiner renders Kohda's cell unsatisfactory for its intended purpose of storing tri-level data.

Second, as is clearly shown by the specific cell design in all of Figs. 3A, 3B, 8, 9, 10 of Kohda, by extending control gate 6 vertically, Kohda achieves source and

drain regions which are self-aligned to the edges of the control gate 6. That is, during manufacturing of the cell, the outer edges of control gate 6 are used to define the source and drain regions. Self-aligned source/drain regions are critical to the proper functioning of the cell, and is required to ensure "a symmetrical configuration with respect to a center line between the impurity regions 2 and 3" (col. 5, lines 63-65). If control gate 6 was reoriented so that it extends over the drain and source regions as suggested by the Examiner, the source and drain regions would no longer be self-aligned to the edges of control gate 6. This would render the "symmetrical configuration" of the cell susceptible to process misalignments.

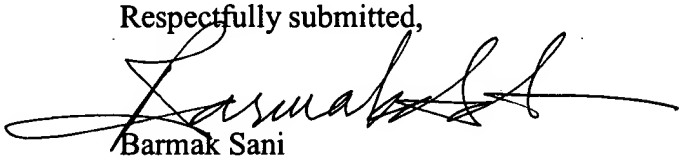
Thus, it is believed that each of claims 1 and 28 and their respective dependent claims distinguish over Kohda and Tigelaar et al. taken singly or in combination at least for the reasons stated above.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



Barmak Sani
Reg. No. 45,068

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 650-326-2400 / Fax: 415-576-0300
BXS:gjs

PA 3283805 v1